OIPE
JUL 11 2005
PATENT & TRADEMARK OFFICE
JC48

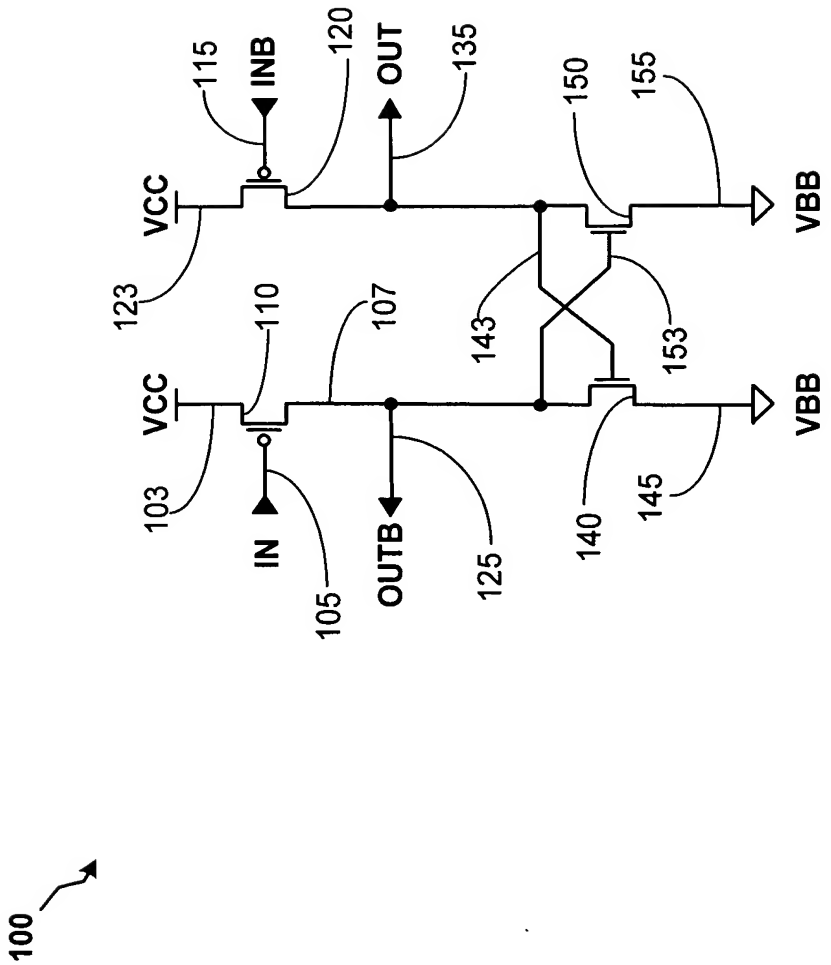


Figure 1 (Prior Art)

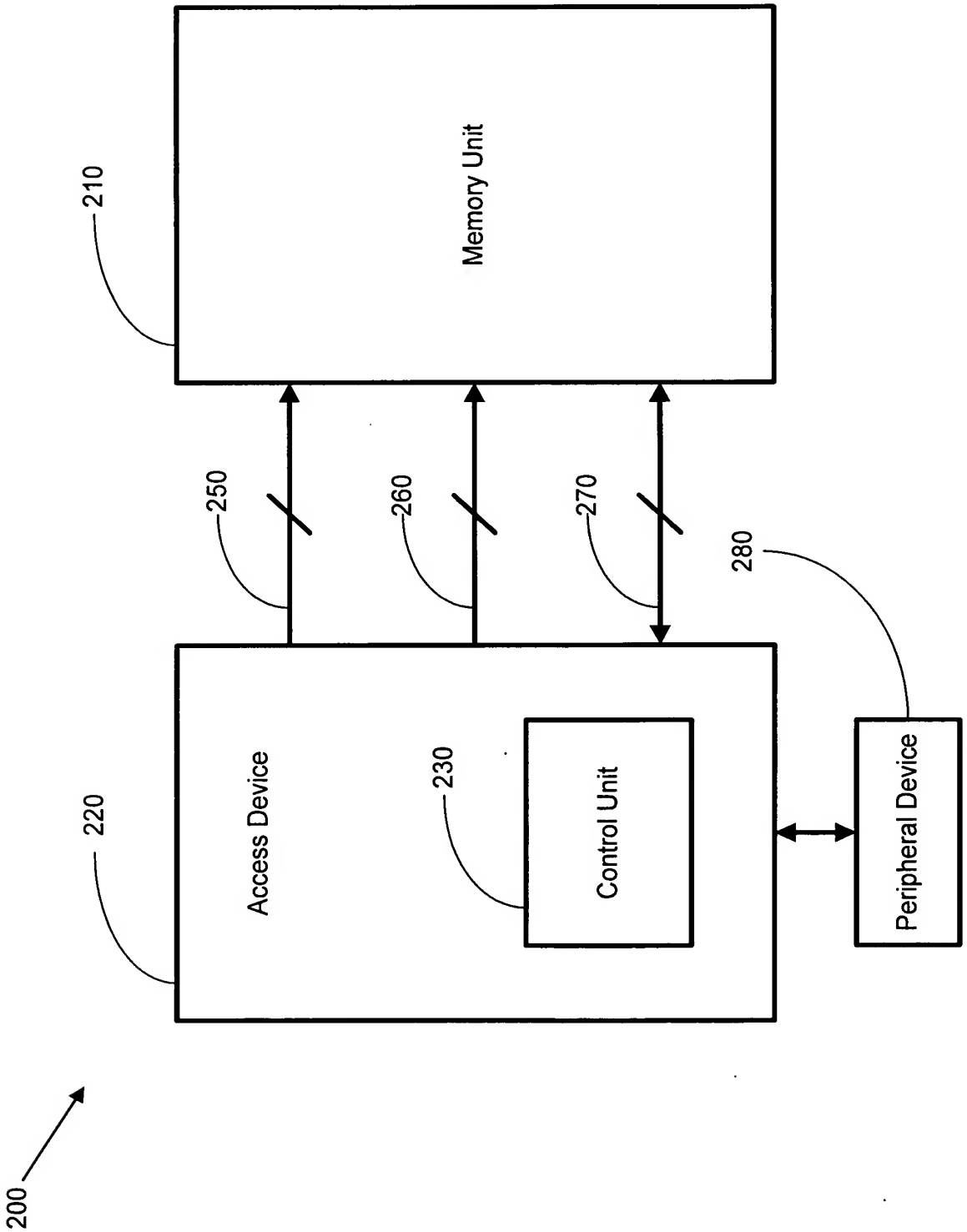

200
210
Memory Unit
250
260
270
280
220
Access Device
230
Control Unit
Peripheral Device

Figure 2

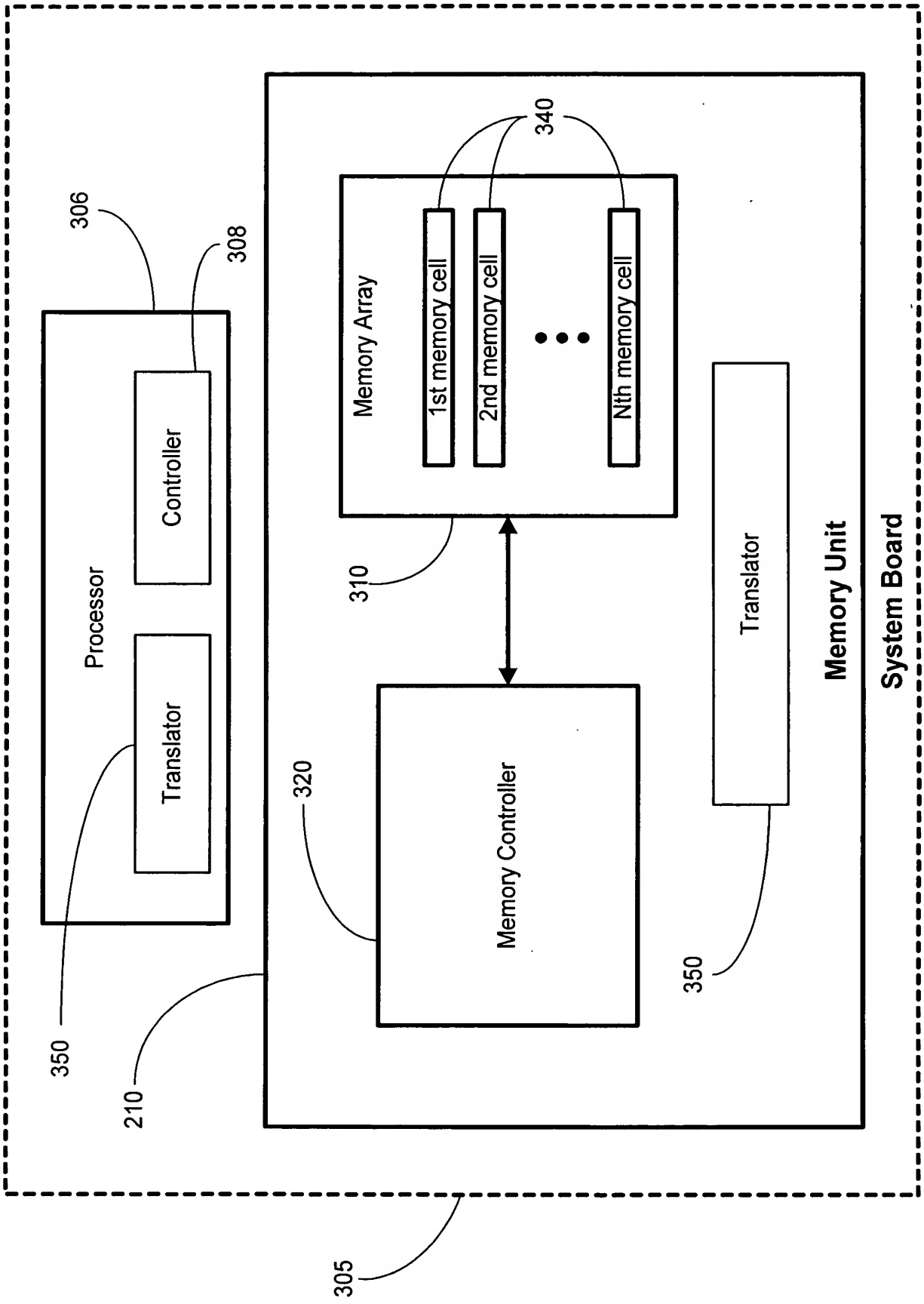

305
System Board
Memory Unit
Processor
306
308
Controller
Translator
350
210
Memory Array
340
1st memory cell
2nd memory cell
Nth memory cell
310
320
Memory Controller
Translator
350

Figure 3

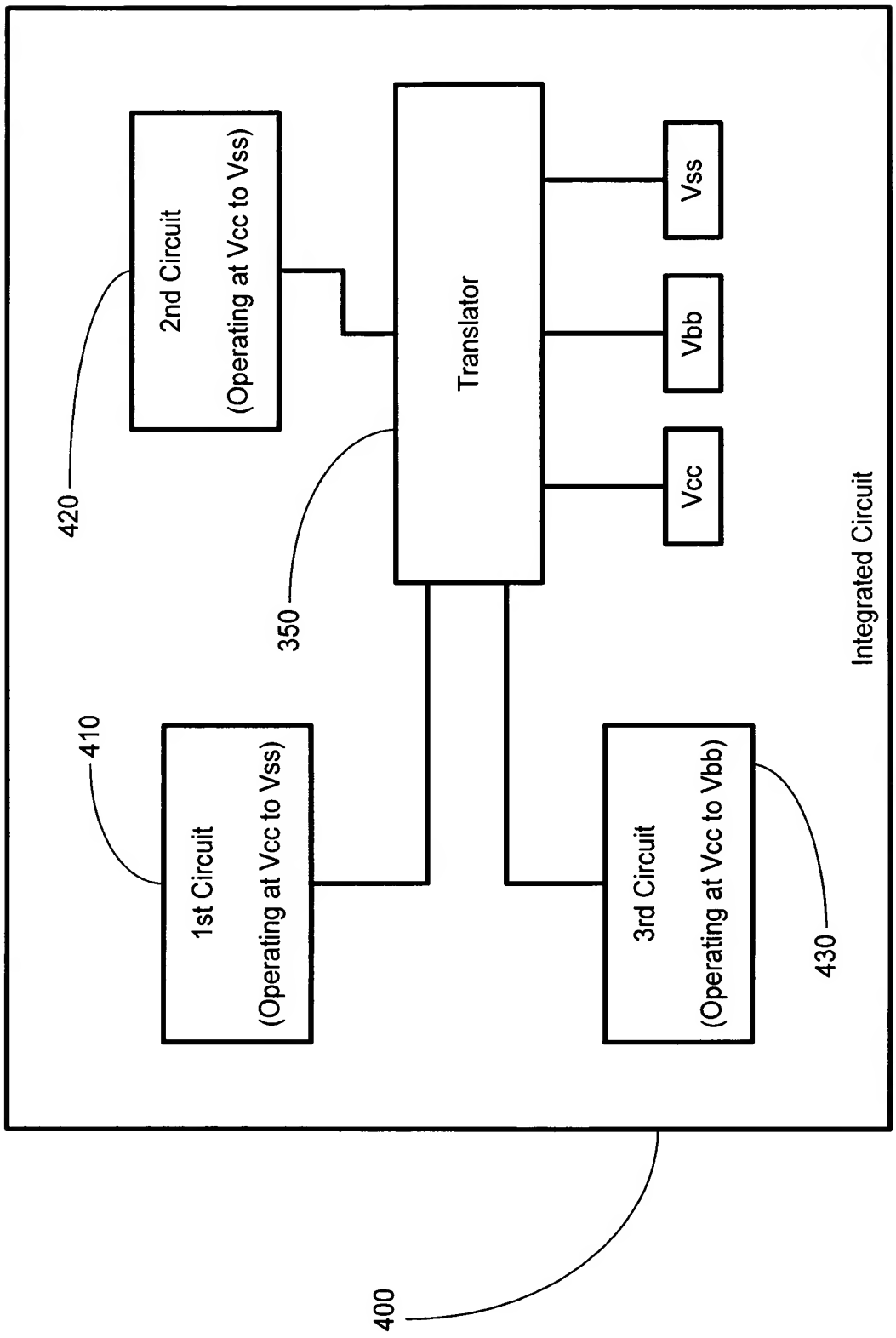
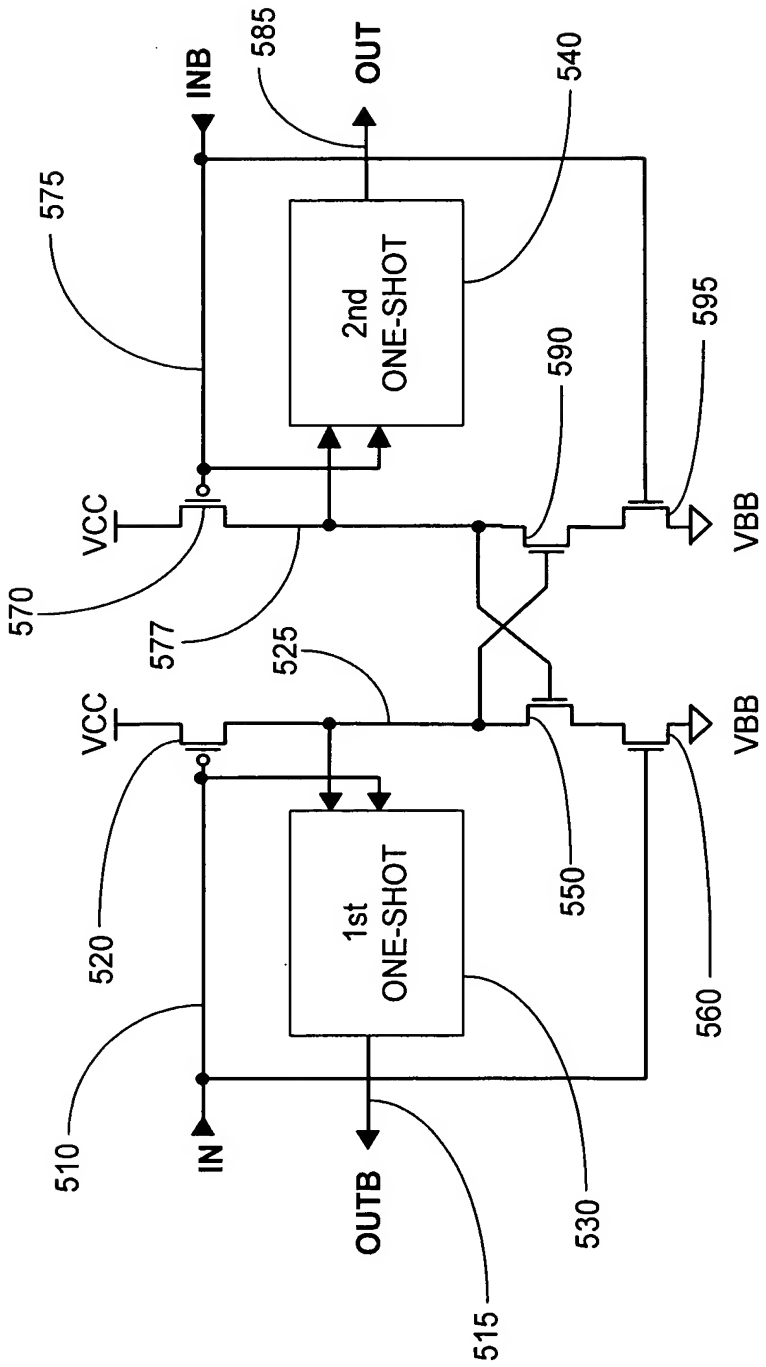


Figure 4
Corrected Sheet



P-Channel Implementation of the Translator

Figure 5

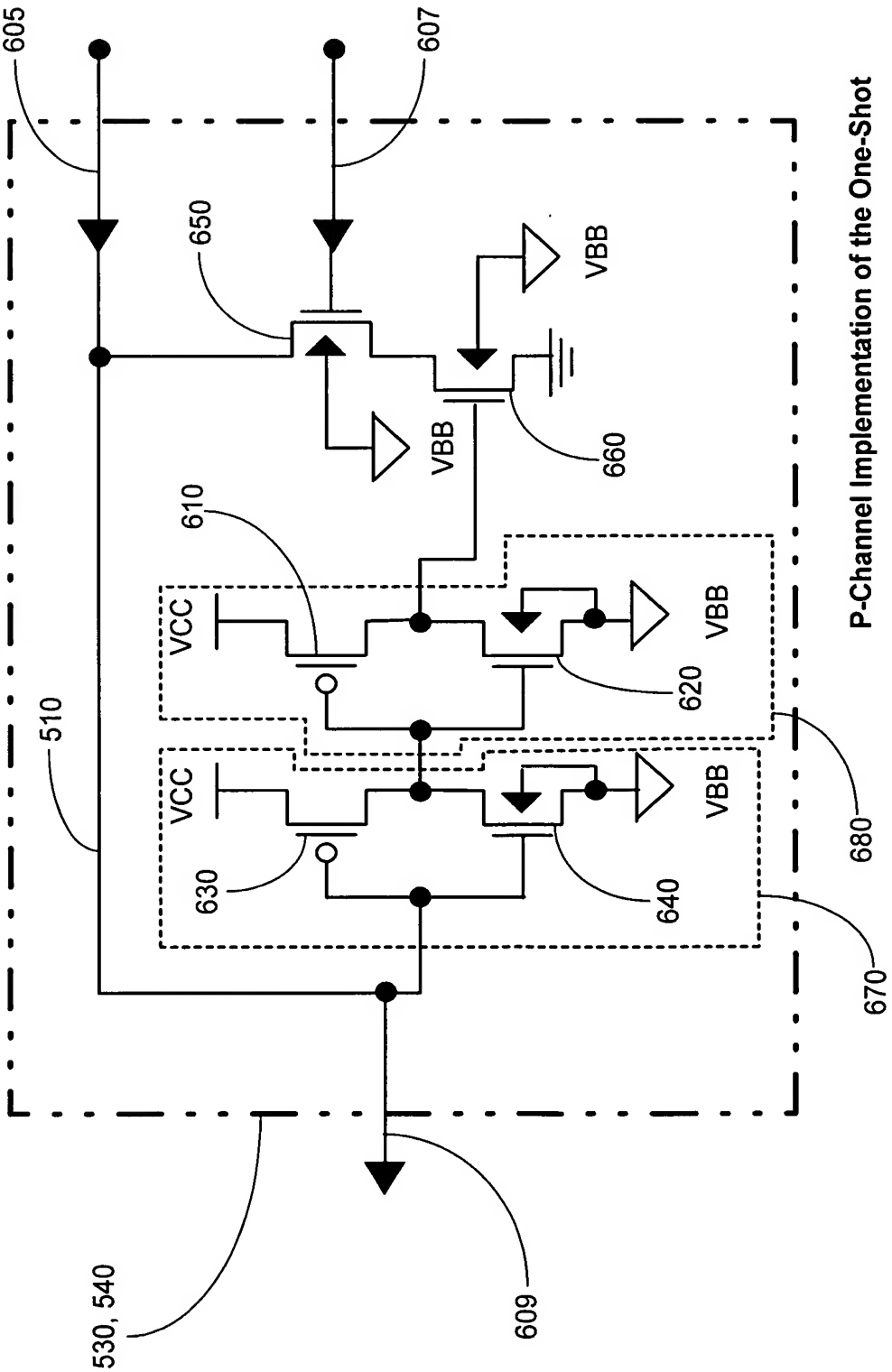
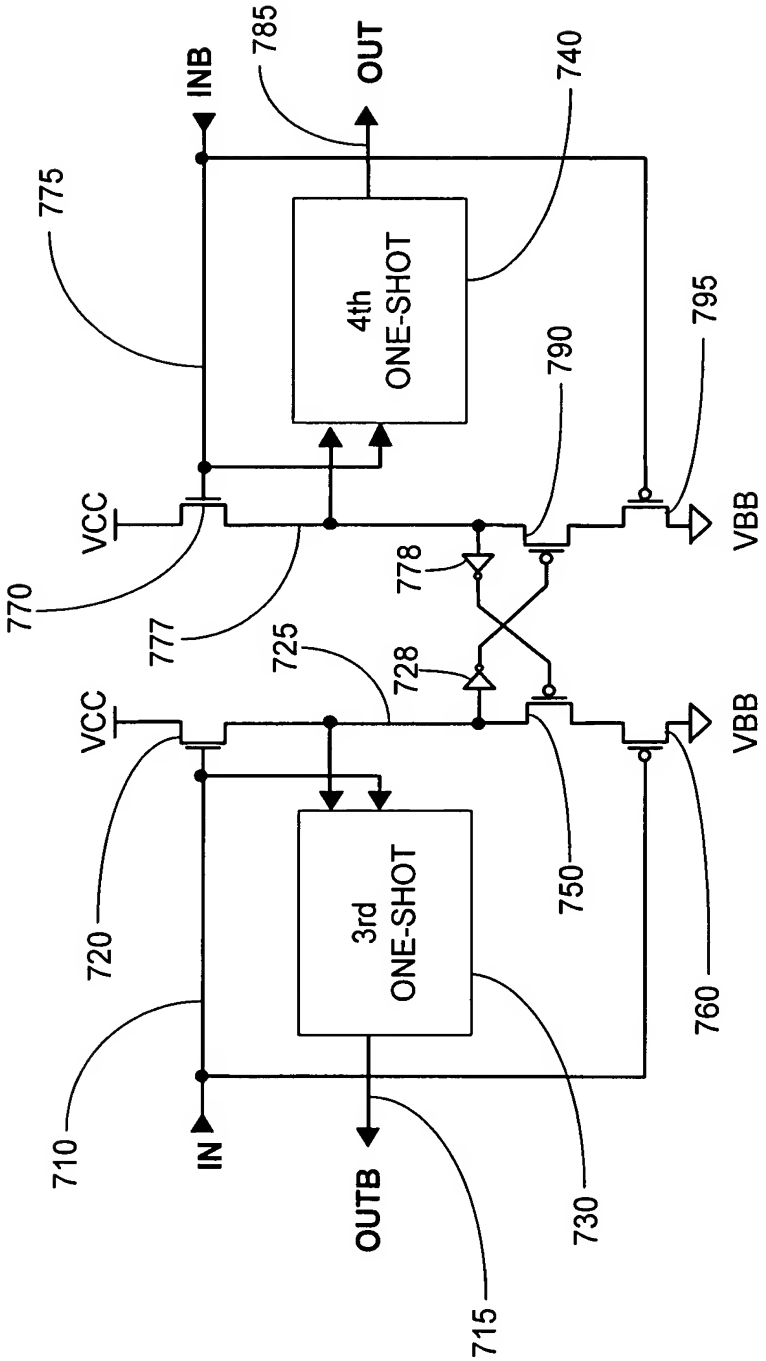
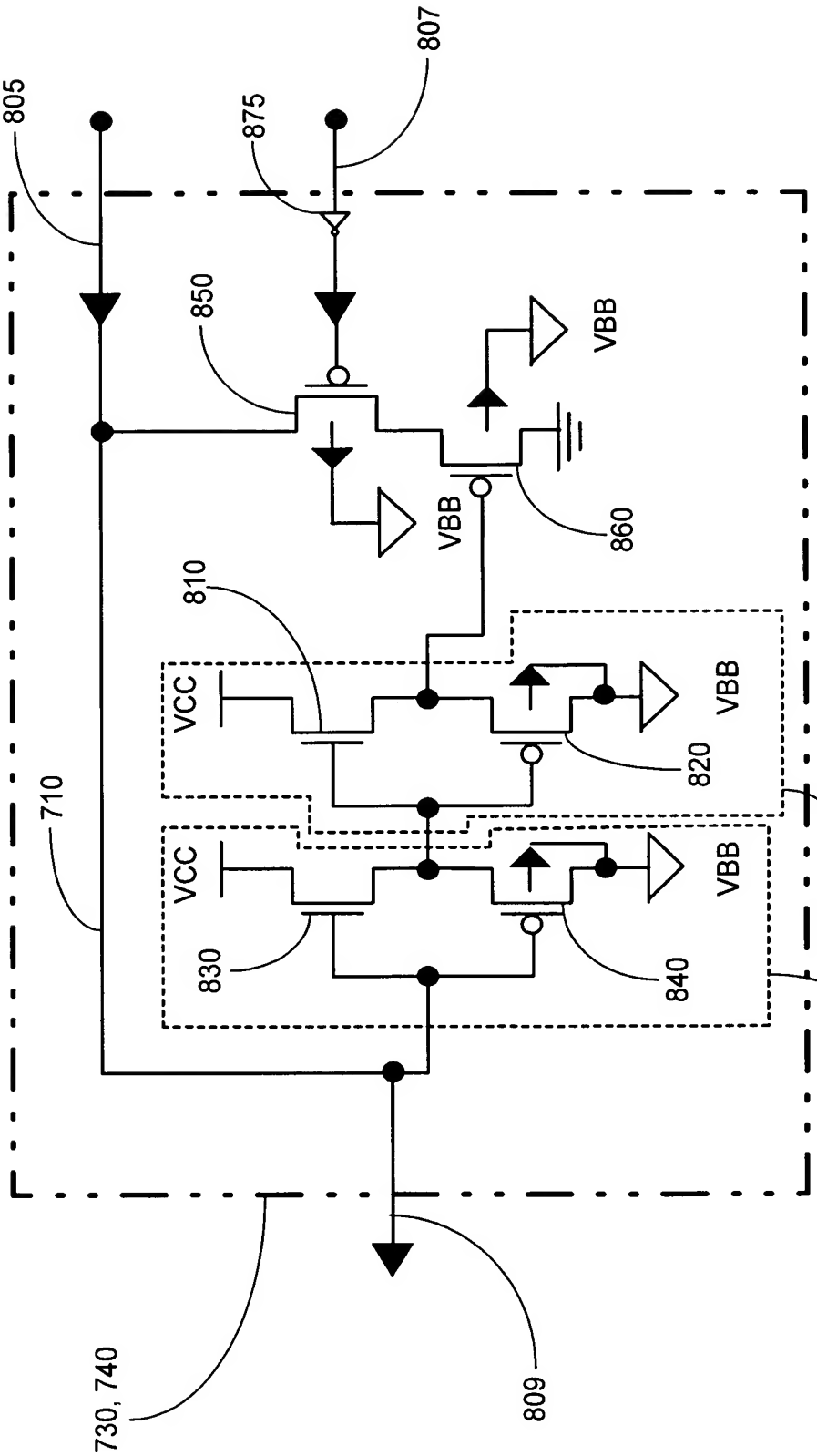

605
607
650
VBB
VBB
660
610
VCC
VBB
620
510
VCC
VBB
630
640
680
670
530, 540
609
P-Channel Implementation of the One-Shot

Figure 6



N-Channel Implementation of the Translator

Figure 7



N-Channel Implementation of the One-Shot

Figure 8